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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	09/931,131
Filing Date	August 16, 2001
First Named Inventor	Hyungwon Kim, et al.
Group Art Unit	2812
Examiner Name	
Attorney Docket Number	UOM 0209 PUSP

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		DAMIANI, MAURIZIO, ET AL, Optimization of Combinational Logic Circuits Based on Compatible Gates, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 11, November 1995.	
		STANION, TED, ET AL, Boolean Division and Factorization Using Binary Decision Diagrams, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 9, September 1994, pgs. 1179-1184.	
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		PAL, AJIT, ET AL, Synthesis of Two-Level Dynamic CMOS Circuits, IEEE, 1999, pgs. 82-92.	
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Examiner Signature		Date Considered	4/23/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.